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18. Okt. 2005
Frist

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Radecker	Docket No.:	INF-141
Serial No.:	10/798,863	Art Unit:	2826
Filed:	March 12, 2004	Examiner:	Kevin V. Quinto

Title: Method for Producing Insulator Structures including a Main Layer and a Barrier Layer

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Affidavit filed under 37 C.F.R. § 1.131

Dear Sir:

I, Joerg Radecker, do hereby state that:

1. I am the sole inventor of the above-reference patent application.

2. Before March 3, 2003, I conceived of and reduced to practice the subject matter of the above-reference patent application.

3. Before March 3, 2003, I signed an invention disclosure form related to the above-reference patent application. A copy of this form is provided herewith as Attachment A (where dates and other material unrelated to proof of invention are masked out).

4. In Attachment A, I describe the present invention and provide micrographs evidencing that this invention was implemented prior to March 3, 2003. The insulator structures depicted in the micrographs were built in Dresden, Germany.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Respectfully submitted,

18 / 10 / 2005
Date

Joerg Radecker

GESAMT SEITEN 01
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Invention Disclosure

Infineon Technologies AG and Affiliated Companies

Please forward in a sealed envelope to a company representative
For company representative in charge of the inventor's department please see:
http://intra.muc.infineon.com/intellectual_property/de/downloads/IP-Contact.pdf

Administrative File Reference: _____

First and last name of the inventor(s):
Further details and signature(s) to be provided on the last page

Jörg Radecker

Number of inventors: 1

Title of the invention:
Enabling of F-based HDP processes on products w/o SiN-liner by implementing protection barriers

Disclosure date: [redacted]

Is the invention publicly funded? (e.g. BMBF, EU-Sponsorship, ...)

☒ no ☐ yes Public project number, title:

Do any related internal R&D projects exist?

☒ no ☐ yes Project:

Did the invention originate from an external project? (e.g. the application history, co-operation, ...)

☒ no ☐ yes Project number, contract number, title:

For the **company's representative** to fill in:

Mr./Ms. Department:

Date of receipt: _____
Beginning of the statutory time limit for further actions within Infineon (examination for completeness within 2 Months, claim period: Germany 4 Months/ Austria 3 Months)

The following documents have been read and the invention described within has been understood:

_____
Representative's signature

Please forward to the IP responsible immediately due to statutory time limits.
For the IP responsible in charge of the inventor's department please see:
http://intra.muc.infineon.com/intellectual_property/de/downloads/IP-Contact.pdf

For the **IP responsible** to fill in:

Mr./Ms. Department

Date of receipt : _____
The inventors are to be informed of incompletion in writing by the company's representative within 2 months from receipt

The following documents have been read, found to be complete and the invention described within has been understood:

_____
IP responsible's signature

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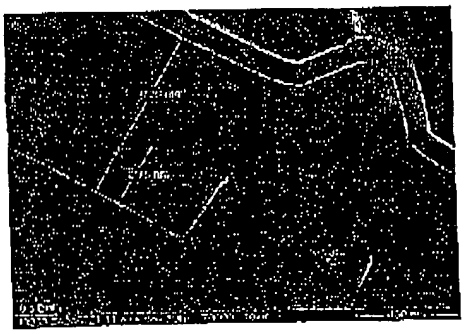
Information on the description of the invention (please fill out your answer below)

1. What technical problem(s) is to be solved by your invention ?
2. How has the problem been solved in prior art?
   What are the disadvantages under the prior art?
3. How does your invention solve this problem and what advantages does this solution offer? (please give a detailed description)
4. What is the core of your invention? (i.e the basic concept of your invention)
5. Please provide precise embodiments and/or implementation examples and select the preferred one for your invention. (Full description, preferably accompanied with drawings)
6. Please attach all documents known to you that contribute to the understanding of your invention as well as to the delimitation over prior art (e.g. publications, patents, copies of lab notebooks etc.)

Research facility under IPAS BUS http://fiz.mchp.siemens.de/IPAS/home/IPAS_BUS.htm

1.) Voidfree gapfill of Isolation Trenches (IT) is one of the most challanging problems within the AA module for technology shrink nodes. Due to the shrinkage the Aspect ratio (AR) will increase. Layout changes will worsening the situation (MINT layout with segmented AA's vs. Checkerboard design with line-space-structures). All known HDP processes with conventional chemistries lead to voids starting at AR~4. Only one HDP based process variant is known which extend the gapfill process window up to AR~6-7 (shown on ARTEMIS VTC structures). An additionally F-based process gas is added during deposition for that processes. With that additionally chemical etching component the redeposition and cusping at the top of the structures will be suppressed and the voidfree bottom up fill is guaranteed.
A problem occurs if products without SIN liner should be processed (is the case for the 90nm DRAM). Due to the interaction of the Fluorine species with the bulk Silicon (direct or via diffusion through AA-oxide and/or undoped HDP-liner) $Si_xF_xO_x$ will be formed and lead subsequent to changed oxide quality (resulting in changed wet etch rates). This defects are clearly seen in BHF-decorated SEM's:



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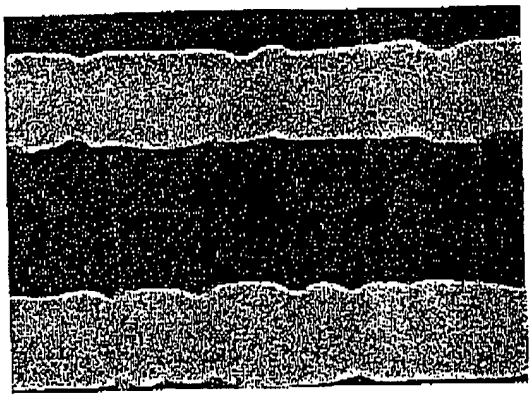
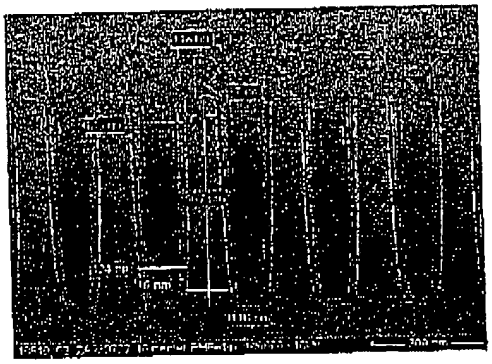
This weak oxide is touched by CMP and/or following wet etch steps and will be filled with GC poly and lead to GC-GC shorts. On the other side reliability problems (QBD) can be the result.



2.) As noticed HDP processes with standard chemistry (Ar, He, H2 addition) reach their limit for voidfree gapfill at AR~4. Strategies to burry the voids down that they won't be opened by CMP are highly risky (especially for fixed abrassive CMP strategies with very long deglaze times).
Descriped problems with the F-based processes do not occur on products with integrated SiN liner (e.g. VTC ARTEMIS):



But SiN liner directly prior the HDP deposition (just after the AA-oxidation) is forbidden for PTC products due to negative influence on p-FET transistor.

3.) By implementing of suitable protection layers within the HDP deposition a barrier against the Fluorine attack is formed. Different materials for that layer are imaginable (e.g. Si-N; a-Si; Si-O-C; ...). All of them are produceable in-situ on the HDP chamber only with changing the gases during the single steps of deposition (highly productive, no interfaces due to contact with atmosphaere).
A typical process flow can be as follow:

Source Plasma HeatUp
first undoped biased deposition (as common for that kind of process)
protection layer (as descriped)
F-based deposition
second undoped biased deposition

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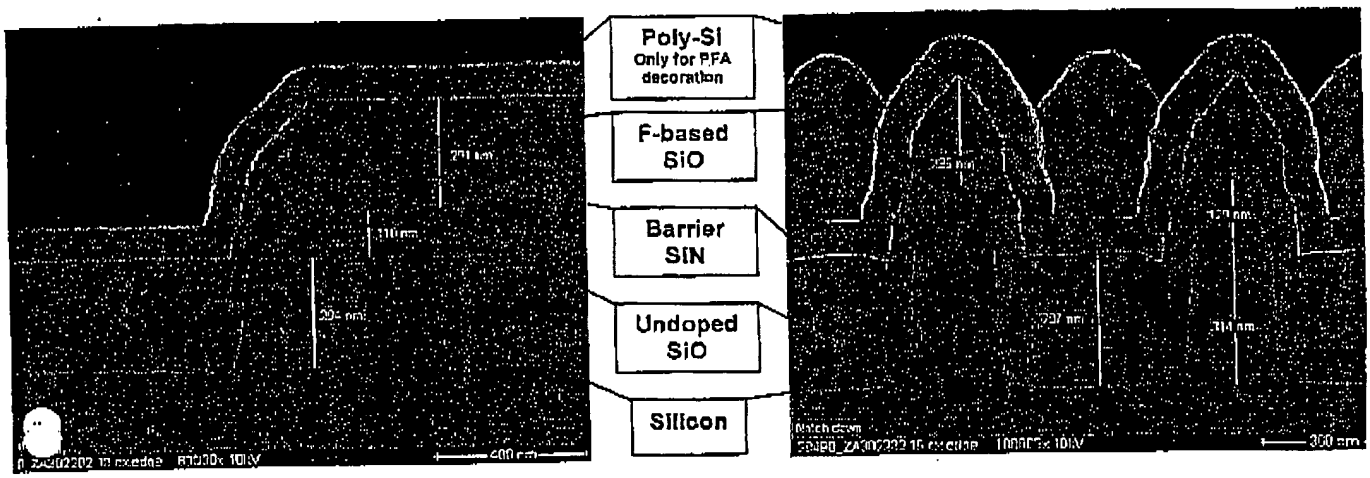
Principle funtioning is shown with an ex-situ deposited Si-N liner:



4.) integrated deposition of barrier liner to prevent Fluorine attack on Si during F-based HDP deposition

5.) Using of any kind of protection layer is neccessary to enabling the usage of F-based HDP processes. For technologies w/o integrated SiN liner (just after the AA-oxidation) a sandwichdeposition (with protection layer after starting with an undoped HDP deposition) will be neccessary. First product will be the 90nm DRAM (target process for STI-fill is F-based HDP).

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Information on the invention

1. What departments are interested in the invention? MDC UPD F / TDT
2. Earliest date as of which onwards the invention was continuously developed [redacted]
3. Has invention disclosure already been submitted on a related subject?

☒ no ☐ yes Invention Disclosure number:

4. Has the invention already been examined (test performance, sample production)?

☐ no ☒ yes Date: [redacted] Results: positive

5. What products is your invention applicable to? all products with deep IT and therefore high AR (e.g. DRAM</=90nm)
6. Is the use of your invention planned?

☐ no ☒ yes When?: [redacted] Where?: 90nm DRAM

7. Has any product been delivered incorporating the invention; is any delivery intended; or has the product incorporating the invention been offered for sale?

☒ no ☐ yes When?: Product name:

8. Has any information relating to the invention been publicly released or is publication intended?

☒ no ☐ yes When?: In book, journal:

9. Is a disclosure of the invention outside the company planned or has a disclosure of the invention outside the company already taken place (reserved or unreserved)?

☒ no ☒ yes When?: [redacted] Where?: [redacted]

10. If yes, have any agreements been concluded or is conclusion intended (e.g. non-disclosure agreement)?

☐ no ☒ yes When?:

Please answer the following questions:

a. Equivalent alternatives to the invention:

- ☒ are practically impossible
- ☐ require considerable effort
- ☐ are viable without any problems

b. A competitor's interest in the invention is:

- ☒ high
- ☐ moderate
- ☐ low

c. To show infringement of the invention by a competitor is:

- ☐ easy
- ☒ difficult
- ☐ nearly impossible

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Personal Information
For more than 4 inventors please use an additional form
(Please name the inventor with whom the attorney shall correspond under number 1!)

1. Inventor	2. Inventor	3. Inventor	4. Inventor
Name:			
Radecker			
Maiden name:			
First name:			
Jörg			
Personnel number: (please see company identification card or pay slip)			
[redacted]			
Academic Degree/Title/Profession:			
Is this your first invention disclosure?			
☒ no ☐ yes	☐ no ☐ yes	☐ no ☐ yes	☐ no ☐ yes
At the time of invention: Were you a student, trainee, graduate student, or PhD student? (please attach a copy of your contract)			
☒ no ☐ yes	☐ no ☐ yes	☐ no ☐ yes	☐ no ☐ yes
Occupation/Position within the company: (e.g. design engineer)			
process engineer			
If Infineon Technologies AG is not your employer, please name your current employer. If any agreements exist that regulate the rights to the invention, please attach a copy of the contract/employment agreement.			
Department: (please give full title)			
MDC UPD F			
Location:			
DD			
Phone/Fax: (including country code)			
++49-351-886-2286			
E-mail:			
joerg.radecker@infineon.com			
Nationality:			
german			
Home Address: (Street and number)			
Baumstr.05			
Zip code and city:			
01099 Dresden			
Date of Birth:			
09/22/1970			
What share of the invention do you hold?			

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100 %	%	%	%
1. Inventor	2. Inventor	3. Inventor	4. Inventor
Has the invention been reported to any other board (e.g. 3i, Infinovate) or authority or is such intended?			
☒ no ☐ yes	☐ no ☐ yes	☐ no ☐ yes	☐ no ☐ yes
Was the invention developed in: a. your field of work? b. a different field of work of your employer?			
☒ a. ☐ b.	☐ a. ☐ b.	☐ a. ☐ b.	☐ a. ☐ b.
Did a problem given to you to solve by your employer lead to the invention?			
☐ no ☒ yes	☐ no ☐ yes	☐ no ☐ yes	☐ no ☐ yes
Do you consider the invention as a releasable invention? (please list your reasons)			
☐ no ☐ yes	☐ no ☐ yes	☐ no ☐ yes	☐ no ☐ yes
Reasons:			

To my/our knowledge no other persons are involved in this invention.
(respective signatures of all inventors)

Jörg Kudelka [redacted]

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